**EXPERIMENT 2**

**Exercise#1:** Design and verify half adder and half subtractor shown in Fig. 1 and Fig. 2 using logisim simulator.

**Half Adder**

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| **Boolean Expressions** | **Logic Diagram** |
| S = A ^ B  C = A B |  |
| **Truth Table** |
|  |

**Half Subtractor**

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| --- | --- |
| **Boolean Expressions** | **Logic Diagram** |
| S = A ^ B  C = A’ B |  |
| **Truth Table** |
|  |

**Exercise#2 :** Design and verify full adder using logisim simulator (i) basic gates only shown in Fig. 3 (ii) by adding half adder (without in-built blocks) as sub circuit similar as shown in Fig. 4.

**Basic Gates Only**

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| --- | --- |
| **Boolean Expressions** | **Logic Diagram** |
| S = A ^ B ^ C  C2 = (A^B) + A B |  |
| **Truth Table** |
|  |

**Adding Half Adder**

|  |  |
| --- | --- |
| **Boolean Expressions** | **Logic Diagram** |
| S =  C = |  |
| **Truth Table** |
|  |

**Exercise#3:** Design 4-bit binary adder using one half adder and 3-full adders as shown in Fig. 5. Use half adder and full adders as sub circuits in the design. Display both the input digits; output digit and end carry digit using Hex digit display with splitter available in logisim simulator.

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| **Logic Diagram** |
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**Exercise#4:** Design 4-bit binary adder-subtractor using full adders as shown in Fig. 6. Use full adders as sub circuits in the design. Display both the input digits, initial carry digit; output digit, and end carry digit using Hex digit display with splitter available in logisim simulator.

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| **Logic Diagram** |
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**Experiment 3**

**Exercise#1:** Design an 8:1 multiplexer (without in-built blocks) using two 4:1 multiplexers and one 2:1 multiplexer (shown in Fig.1) Use both types of multiplexers as sub circuits in the design.

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| **Logic Diagram** |
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**Exercise#2:** Design a 1:8 de-multiplexer (without in-built blocks) using three 1:4 de-multiplexers. Use 1:4 de-multiplexers as sub circuits in the design.

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| **Logic Diagram** |
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**Exercise#3**: Design quad to binary (4-to-2) encoder (without in-built blocks) using logic gates. Display all four input digits using seven segment displays and two output binary bits using hex displays available in logisim simulator

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| **Logic Diagram** |
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**Exercise#4:** Design 3-to-8 decoder (without in-built blocks) using two 2-to-4 decoders with enable (E) line shown in Fig. 2. Use 2:4 decoder as sub circuits in the design.

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| **Logic Diagram** |
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